



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/910,554	07/20/2001	Amit Gur	SC0339WI	3496
23125	7590	02/10/2005	EXAMINER	
FREESCALE SEMICONDUCTOR, INC. LAW DEPARTMENT 7700 WEST PARMER LANE MD:TX32/PL02 AUSTIN, TX 78729			BUEHL, BRETT J	
		ART UNIT	PAPER NUMBER	
			2183	

DATE MAILED: 02/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/910,554	GUR ET AL.	
	Examiner	Art Unit	
	Brett J Buehl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 7/20/01, 8/20/01.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-15 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-15 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 20 July 2001 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>8/20/01</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

1. Claims 1-15 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Declaration and Fees as received on 7/20/01, and IDS as received on 8/20/01.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.
4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "60" has been used to designate both decode logic, as in Figure 3, and a shifter/combiner, as in Figure 1. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be

labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

6. Claim 14 is objected to because of the following informalities: Claim 14 recites the limitation, “The circuit of 12”. This limitation should be amended to read as, “The circuit of claim 12”, to more clearly state the claim’s dependency. Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
8. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
9. Claim 12 recites the limitation “a second arrangement means coupled to the second subset for placing the transfer bits contained in the second subset on the first side of the first arrangement means”. This limitation is indefinite, as it is unclear to the examiner if the aligned bits of the second subset are placed in the first arrangement means or the second arrangement means. The examiner will interpret this claim to

indicate the aligned second subset is placed in the second arrangement means (see 44 of Figure 1).

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Laurenti et al., U.S. Patent No. 6,760,837.

12. Regarding claim 1, Laurenti has taught a method for transferring a plurality of bits from a source register to a destination register [Figure 13], comprising the steps of:

- a. Loading the source register with the plurality of bits [916 of Figure 13, It is inherent that the source 2 register is loaded with a plurality of bits, the plurality of bits representing the data on which to operate];
- b. Dividing the source register into a plurality of first level subsets [col. 17, lines 66-67 and col. 18, lines 1-3];
- c. Identifying the bits in each subset which are to be transferred to the destination register [col. 11, lines 49-51], wherein the subsets each have a number of transfer data bits and non-transfer data bits [col. 18, lines 1-3, the portion of the bit mask associated with a subset determines the number of bits to be transferred and the number of bits not to be transferred (indicated by 1's and 0's, respectively)];

d. Aligning the transfer data bits in each first level subset to a first side thereof to form corresponding second level subsets of the transfer data bits [Figure 14, the encoder aligns the first level subset to the right, in logical order];

e. Loading the transfer data bits from the second level subsets into the destination register aligned to the first side of the destination register [col. 18, lines 22-24].

13. Regarding claim 2, Laurenti has taught the method of claim 1 further comprising combining pairs of the first level subsets [1314 of Figure 13 and col. 18, lines 6-9], each pair comprising a first of the pair [1306 of Figure 13] and a second of the pair [1308 of Figure 13], by level shifting the transfer data bits of the first of the pairs and combining the level-shifted transfer bits with the second of the pairs [Figure 15, A7-A4 are from the first of the pair and A3-A0 are from the second of the pair, these bits being shifted and combined].

14. Regarding claim 3, Laurenti has taught the method of claim 2, wherein the step of combining pairs is further characterized as level-shifting the transfer bits of the pairs by an amount equal to the number of non-transfer bits of the first level subset which corresponds to the second of the pair [Figure 15, Table 1 below shows the output of the 1st level selector corresponding to the number of transfer bits in the second subset of the pair (i.e. if there are no transfer bits in the second subset, meaning 4 non-transfer bits, the data in the first subset is shifted 4 positions)].

Table 1: Output table for 1st level selector (Figure 15)

NO	1502a	1502b	1502c	1502d	1502e	1502f	1502g	1502h
----	-------	-------	-------	-------	-------	-------	-------	-------

0	0	0	0	0	A7	A6	A5	A4
1	0	0	0	A7	A6	A5	A4	A0
2	0	0	A7	A6	A5	A4	A1	A0
3	0	A7	A6	A5	A4	A2	A1	A0
4	A7	A6	A5	A4	A3	A2	A1	A0

15. Regarding claim 4, Laurenti has taught the method of claim 3, wherein the step of aligning is further characterized as aligning the transfer bits in a logic order [Figure 14, the bits are shifted in logical order (i.e. higher logical bit positions always on the left of lower logical bit positions)].

16. Regarding claim 5, Laurenti has taught the method of claim 4, wherein the step of combining is further characterized as combining the transfer bits in the logic order [see Table 1 above (i.e. higher logical bit positions always on the left of lower logical bit positions)].

17. Regarding claim 6, Laurenti has taught the method of claim 1, wherein the number of non-transfer bits for at least one of the subsets is zero [col. 19, lines 57-67 and col. 20, lines 10-21, the mask indicates that the first subset (i.e. far left side) has zero non-transfer bits, indicated by all 1's].

18. Regarding claim 7, Laurenti has taught a method for manipulating a plurality of bits from a source register to a destination register, comprising the steps of:

- a. Loading the source register with the plurality of bits [916 of Figure 13, It is inherent that the source 2 register is loaded with a plurality of bits, the plurality of bits representing the data on which to operate];
- b. Dividing the source register into a plurality of first level subsets [col. 17, lines 66-67 and col. 18, lines 1-3];

- c. Identifying the bits in each subset which are to be transferred to the destination register [col. 11, lines 49-51], wherein the subsets are in logic order [916 of Figure 13, the subsets are in logical order, the first subset representing bits A15-A12, etc.] and each have transfer data and non-transfer data [col. 18, lines 1-3, the portion of the bit mask associated with a subset determines the number of bits to be transferred and the number of bits not to be transferred (indicated by 1's and 0's, respectively)];
- d. Aligning the transfer data in each first level subset to a first side thereof to form second level subsets in logic order [Figure 14, the encoder aligns the first level subset to the right, in logical order];
- e. Forming first adjoining pairs of second level subsets each having a second level subset on the first side and a second level subset on a second side [1314 and 1316 of Figure 13, the outputs of 1306 and 1308 are the second level subsets which are adjoined by 1314, and the outputs of 1310 and 1312 are the second level subsets adjoined by 1316];
- f. Combining the first adjoining pairs by shifting the data of each of the second level subsets on the second side to the first side by an amount equal to the number of non-transfer bits in the second level subset on the first side to form third level subsets [Figure 15, Table 1 above shows the outputs of 1314 and 1316 correspond to the number of transfer bits in the second subset of the pair (i.e. if there are no transfer bits in the second subset, meaning 4 non-transfer bits, the data in the first subset is shifted 4 positions), the third level subsets are the outputs from 1314 and 1316];

g. Forming second adjoining pairs of third level subsets each having a third level subset on the first side and a third level subset on the second side [Table 8 (col. 19) and Figure 15, 1322 adjoins pairs of third level subsets];

h. Combining the second adjoining pairs by shifting the data of each of the third level subsets on the second side to the first side by an amount equal to the number of non-transfer bits in the third level subset on the first side to form fourth level subsets [1322 of Figure 13, Table 2 below shows that the 2nd level selector takes as inputs the third level subsets, and then shifts and combines the subsets (see Table 2). The left column indicates the number of transfer bits of the subset on the right, meaning the amount of the shift is actually equal to the number of non-transfer bits of the subset on the right (i.e. if there are 3 bits to be transferred from the subset on the right, then the data from the left subset is shifted right by 5 bits)];

Table 2: Output table for 2nd level selector (Figure 15)

	O15	O14	O13	O12	O11	O10	O9	O8	O7	O6	O5	O4	O3	O2	O1	O0
0	0	0	0	0	0	0	0	0	A15	A14	A13	A12	A11	A10	A9	A8
1	0	0	0	0	0	0	0	A15	A14	A13	A12	A11	A10	A9	A8	A0
2	0	0	0	0	0	0	A15	A14	A13	A12	A11	A10	A9	A8	A1	A0
3	0	0	0	0	0	A15	A14	A13	A12	A11	A10	A9	A8	A2	A1	A0
4	0	0	0	0	A15	A14	A13	A12	A11	A10	A9	A8	A3	A2	A1	A0
5	0	0	0	A15	A14	A13	A12	A11	A10	A9	A8	A4	A3	A2	A1	A0
6	0	0	A15	A14	A13	A12	A11	A10	A9	A8	A5	A4	A3	A2	A1	A0
7	0	A15	A14	A13	A12	A11	A10	A9	A8	A6	A5	A4	A3	A2	A1	A0
8	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

i. Loading the transfer data from the fourth level subsets into the destination register in consecutive order aligned to the first side of the destination register [1324 of Figure 13, the output from the 2nd level selector, which is comprised of

the fourth level subsets, is the input to the destination register. All of the operations (i.e. the shifting) has been in logical order, meaning the output from 1324 is still in logical order (see Tables 1 and 2, above)].

22. Regarding claim 8, Laurenti has taught a circuit comprising:
 - a. A source register with the plurality of bits divided into a plurality of first level subsets [916 of Figure 13, col. 17, lines 66-67 and col. 18, lines 1-3];
 - b. Means for identifying the bits in each subset which are transfer bits and non-transfer bits [col. 11, lines 49-51];
 - c. Arranger means for aligning the transfer data bits in each first level subset to a first side thereof to form corresponding second level subsets of the transfer data bits [1306 of Figure 13 and Figure 14, the encoder aligns the first level subset to the right, in logical order];
 - d. A destination register [1326 of Figure 13] and
 - e. Coupling means for loading the transfer data bits from the second level subsets into the destination register aligned to the first side of the destination register [1322 of Figure 13, the 2nd level selector couples the transfer data to the destination register.].
23. Regarding claim 9, Laurenti has taught the circuit of claim 8 further comprising a combiner means for combining pairs of the second level subsets [1314 and 1316 of Figure 13], each pair comprising a first of the pair and a second of the pair [1306 and 1308 of Figure 13], by shifting the transfer data bits of the first of the pairs to form shifted transfer bits and combining said shifted transfer bits with the second of the pairs [See Table 1, above].

24. Regarding claim 10, Laurenti has taught the circuit of claim 9, wherein the arranger means comprises a plurality of arrangers each for a receiving a set of mask bits [1306, 1308, 1310 and 1312 of Figure 13], each set of mask bits corresponding to one of the arrangers [col. 18, lines 1-3], each arranger corresponding to a subset of the first level subsets [col. 17, lines 66-67 and col. 18, line 1], each arranger comprising: a first multiplexer having a first input coupled to receive a first bit from the subset of the first level subsets to which the arranger corresponds, a second input coupled to receive a second bit from the subset of the first level subsets to which the arranger corresponds, a control input for receiving a first mask bit from the set of mask bits to which the arranger corresponds, and an output; a second multiplexer having a first input to receive the first bit, a second input coupled to the output of the first multiplexer, a control input for receiving a second mask bit from the set of mask bits to which the arranger corresponds, and an output; a third multiplexer having a first input coupled to the output of the first multiplexer, a second input coupled a third bit from the subset of the first level subsets to which the arranger corresponds, a control input for receiving the second mask bit, and an output; a fourth multiplexer having a first input coupled to the output of the third multiplexer, a second input coupled a fourth bit from the subset of the first level subsets to which the arranger corresponds, a control input for receiving a third mask bit from the set of mask bits to which the arranger corresponds, and an output as a first output of the arranger; a fifth multiplexer having a first input coupled to the output of the third multiplexer, a second input coupled to the output of the second multiplexer, a control input for receiving the third mask bit, and an output as a second output of the arranger; and a sixth multiplexer having a first input coupled to the output of the second

multiplexer, a second input coupled to receive the first bit, a control input for receiving the third mask bit, and an output as a third output of the arranger [Figure 14, the functionality of Laurenti's encoder is the same as the arranger].

25. Regarding claim 11, Laurenti has taught the circuit of claim 9, wherein each combiner means comprises: a first plurality of multiplexers coupled to the first of the pair and a first mask signal; a second plurality of multiplexers coupled to the first plurality of multiplexers and a second mask signal; and a third plurality of multiplexers coupled to the second plurality of multiplexers and a third mask signal [Figure 15 and Table 2 (above), the functionality of Laurenti's level-shifter is the same as the combiner/shifters].

26. Regarding claim 12, Laurenti has taught a circuit, comprising:

- a. A source register having a plurality of bits and for containing transfer and non-transfer data contained in first and second subsets of the plurality of bits [916 of Figure 13];
- b. A destination register [1326 of Figure 13];
- c. A first arrangement means coupled to the first subset for placing the transfer bits contained in the first subset on a first side of the first arrangement means [1308 of Figure 13 (see Figure 14 for shifting table)];
- d. A second arrangement means coupled to the second subset for placing the transfer bits contained in the second subset on the first side of the second arrangement means [1306 of Figure 13 (see Figure 14 for shifting table)];
- e. Shifter/combiner means for shifting the data in the second arrangement means toward the first side of the shifter/combiner means by an amount equal to the number of non-transfer bits in the first subset [1314 of Figure 15, Table 1

above shows the output of the 1st level selector corresponding to the number of transfer bits in the first subset of the pair (i.e. if there are no transfer bits in the first subset, meaning 4 non-transfer bits, the data in the second subset is shifted 4 positions)]; and

f. Coupling means for coupling the contents of the first and second means into the destination register [1322 of Figure 13, the 2nd level selector couples the outputs of the 1st level selectors into the destination register (1326 of Figure 13)].

27. Regarding claim 13, Laurenti has taught the circuit of claim 12, wherein the coupling means is further characterized as coupling the contents of the first and second means into the first side of the destination register [col. 19, lines 62-67 and col. 20, lines 10-21, the transfer bits of the first and second subsets are coupled to the destination register, aligned to the right].

28. Regarding claim 14, Laurenti has taught the circuit of 12, wherein the first arrangement means comprises: a first multiplexer having a first input coupled to receive a first bit from the first subset, a second input coupled to receive a second bit from the first subset, a control input for receiving a first mask bit, and an output; a second multiplexer having a first input to receive the first bit, a second input coupled to the output of the first multiplexer, a control input for receiving a second mask bit, and an output; a third multiplexer having a first input coupled to the output of the first multiplexer, a second input coupled a third bit from the first subset, a control input for receiving the second mask bit, and an output; a fourth multiplexer having a first input coupled to the output of the third multiplexer, a second input coupled a fourth bit from the first subset, a control input for receiving a third mask, and an output as a first output of the first arrangement

means; a fifth multiplexer having a first input coupled to the output of the third multiplexer, a second input coupled to the output of the second multiplexer, a control input for receiving the third mask bit, and an output as a second output of the arrangement means; and a sixth multiplexer having a first input coupled to the output of the second multiplexer, a second input coupled to receive the first bit, a control input for receiving the third mask bit, and an output as a third output of the arrangement means [Figure 14, the functionality of Laurenti's encoder is the same as the arranger].

29. Regarding claim 15, Laurenti has taught the circuit of claim 12, wherein the shifter/combiner means comprises: a first plurality of multiplexers coupled to the second arrangement means and a first mask signal; a second plurality of multiplexers coupled to the first plurality of multiplexers and a second mask signal; and a third plurality of multiplexers coupled to the second plurality of multiplexers and a third mask signal [Figure 15 and Table 2 (above), the functionality of Laurenti's level-shifter is the same as the combiner/shifters].

Conclusion

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of art disclosed by the references cited and the objections made. Applicant must show how the amendments avoid such references and objections. See 37 CFR 1.111(c).

31. Inquiries concerning this communication or earlier communications from the examiner should be directed to Brett J. Buehl who can be reached at (571) 272-4161 or

Art Unit: 2183

<brett.buehl@uspto.gov>. The examiner's normal working schedule is between the hours 9:00am – 6:30pm (EST), Monday – Friday, with alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan, can be reached at (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

32. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100